Figure1a (Prior Art)

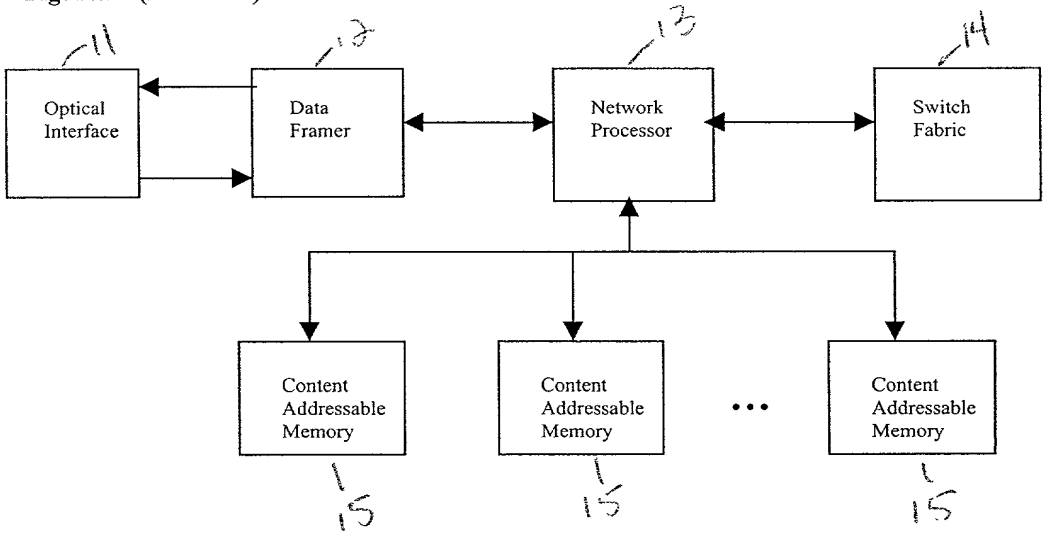

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Figure 1b (Prior Art)

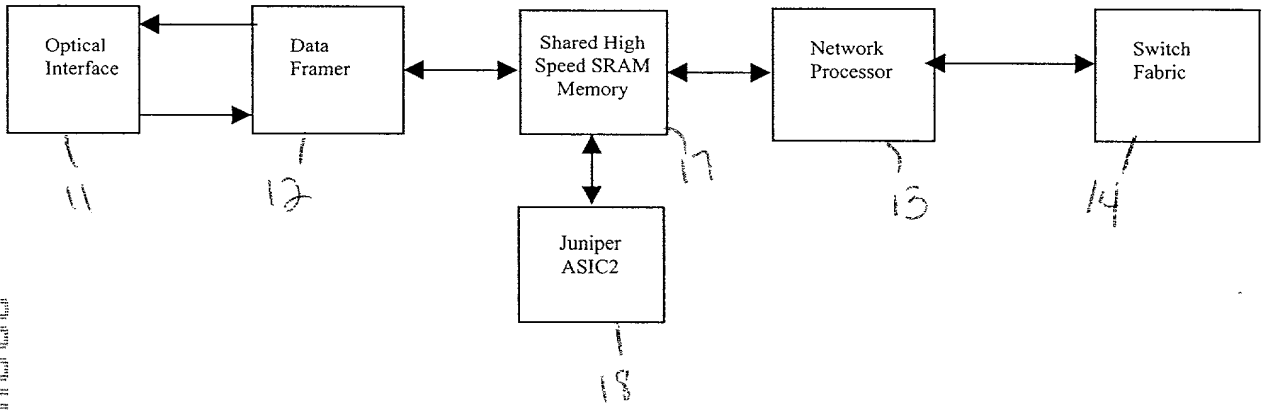

Figure 2A

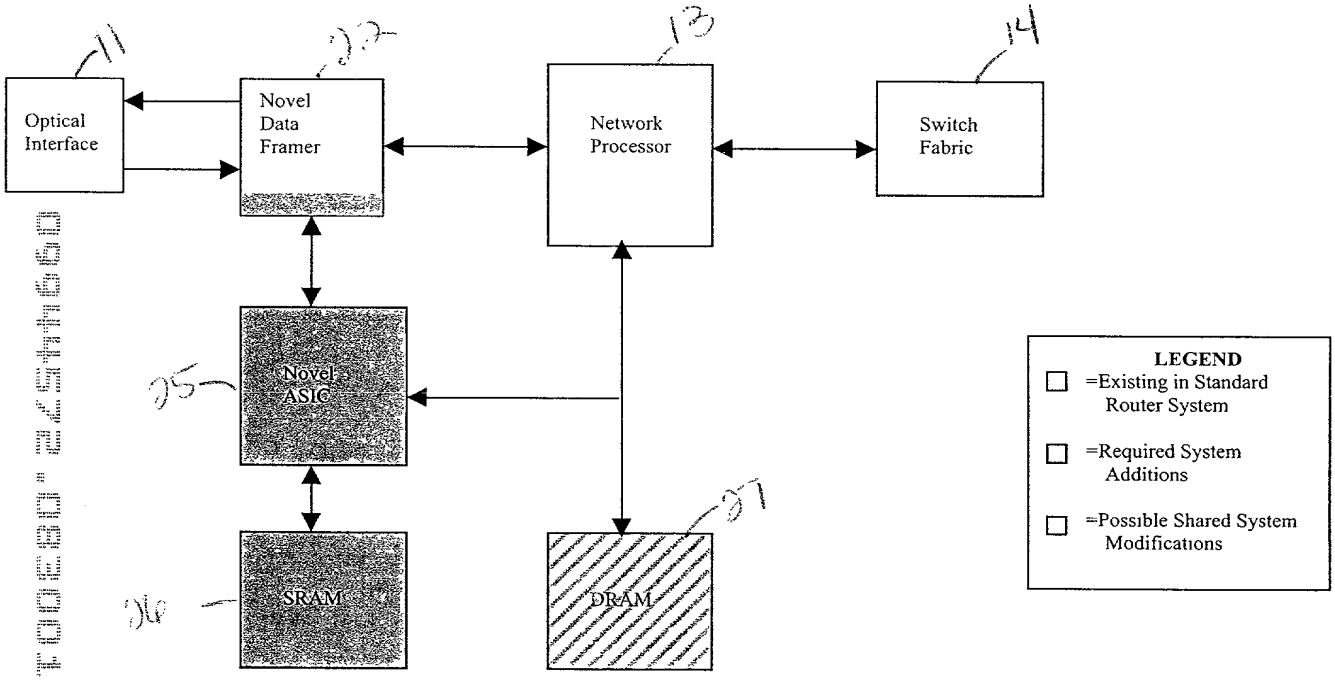
11
12
13
14
Optical Interface
Novel Data Framer
Network Processor
Switch Fabric
25
Novel ASIC
SRAM
DRAM
LEGEND
=Existing in Standard Router System
=Required System Additions
=Possible Shared System Modifications

Figure 2B

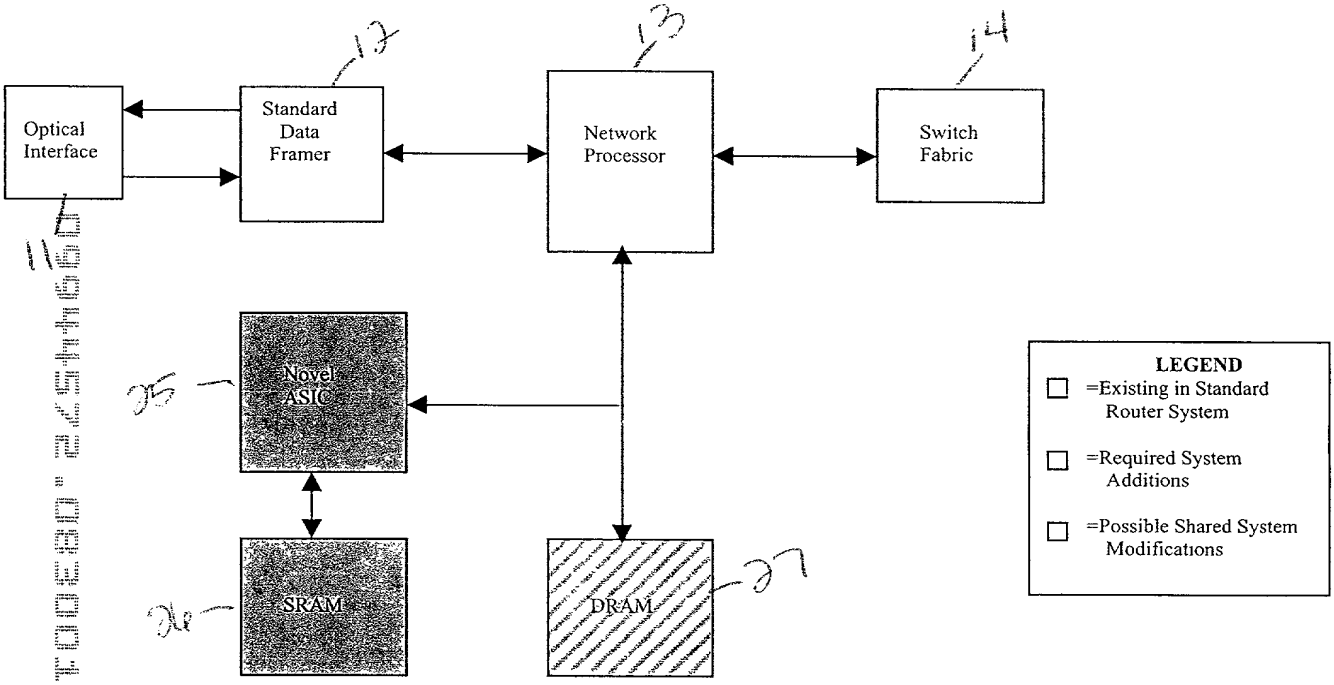
Optical Interface
Standard Data Framer
Network Processor
Switch Fabric
Novel ASIC
SRAM
DRAM
LEGEND
=Existing in Standard Router System
=Required System Additions
=Possible Shared System Modifications

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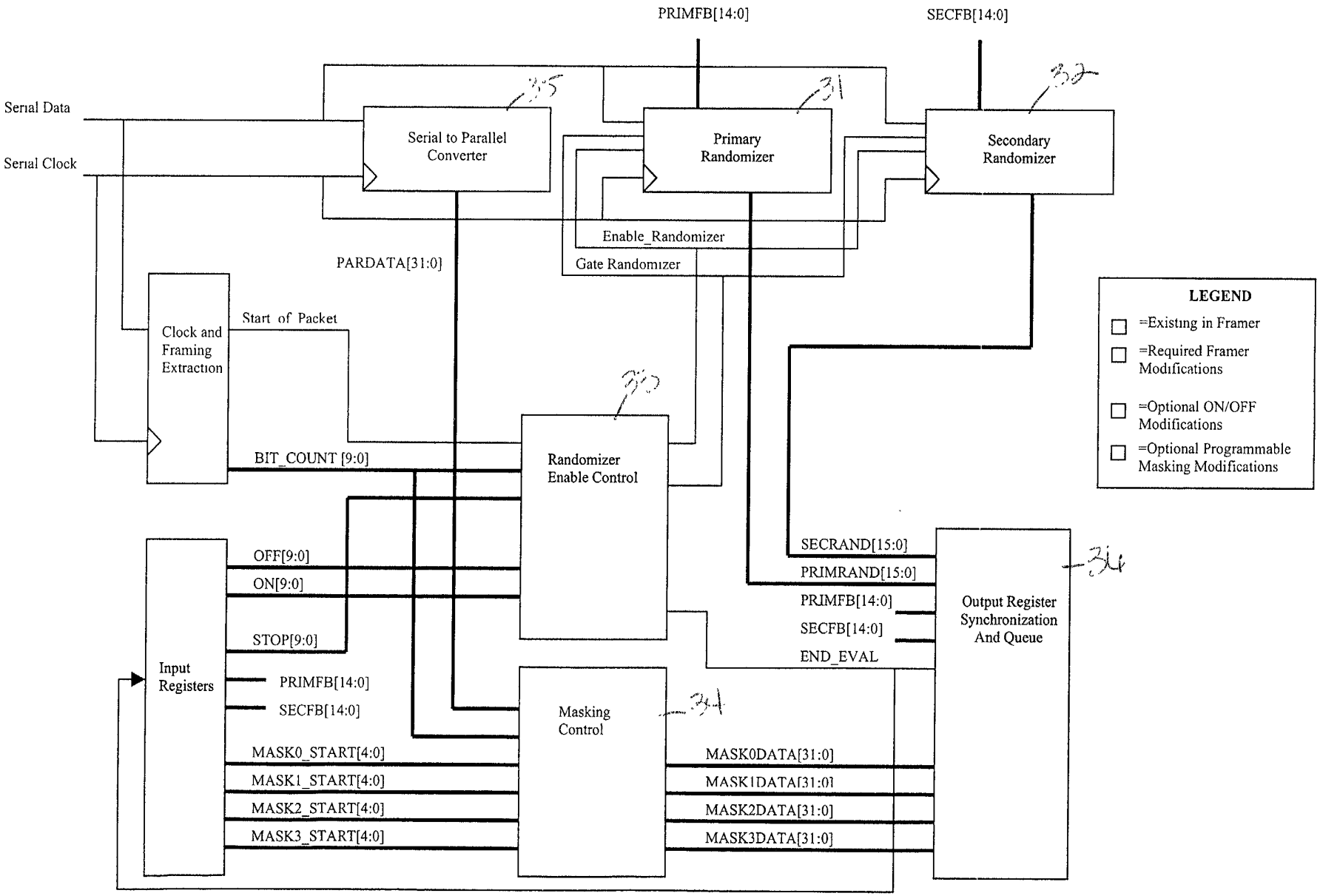
FIGURE 3



22

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FIGURE 4

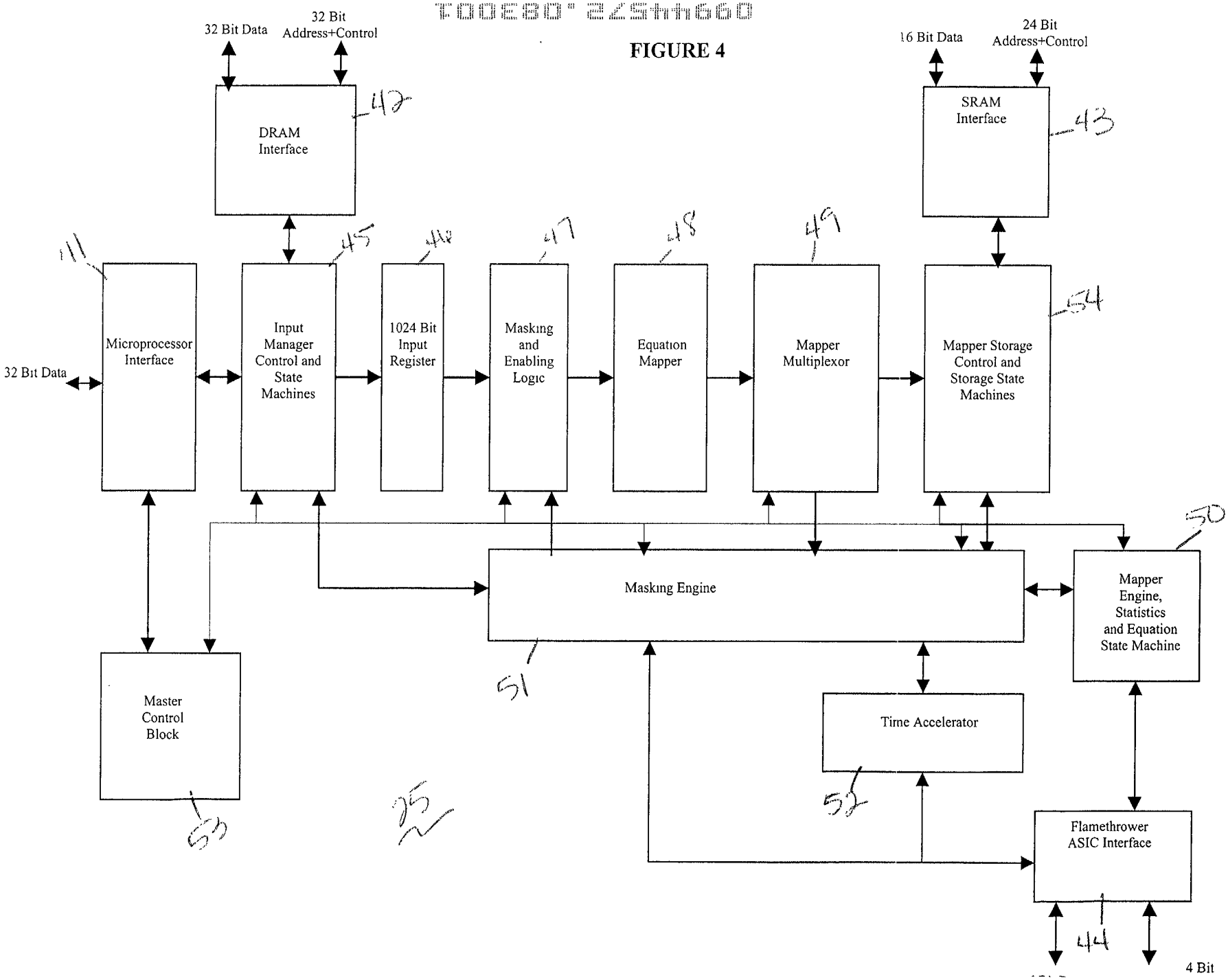


FIGURE 5

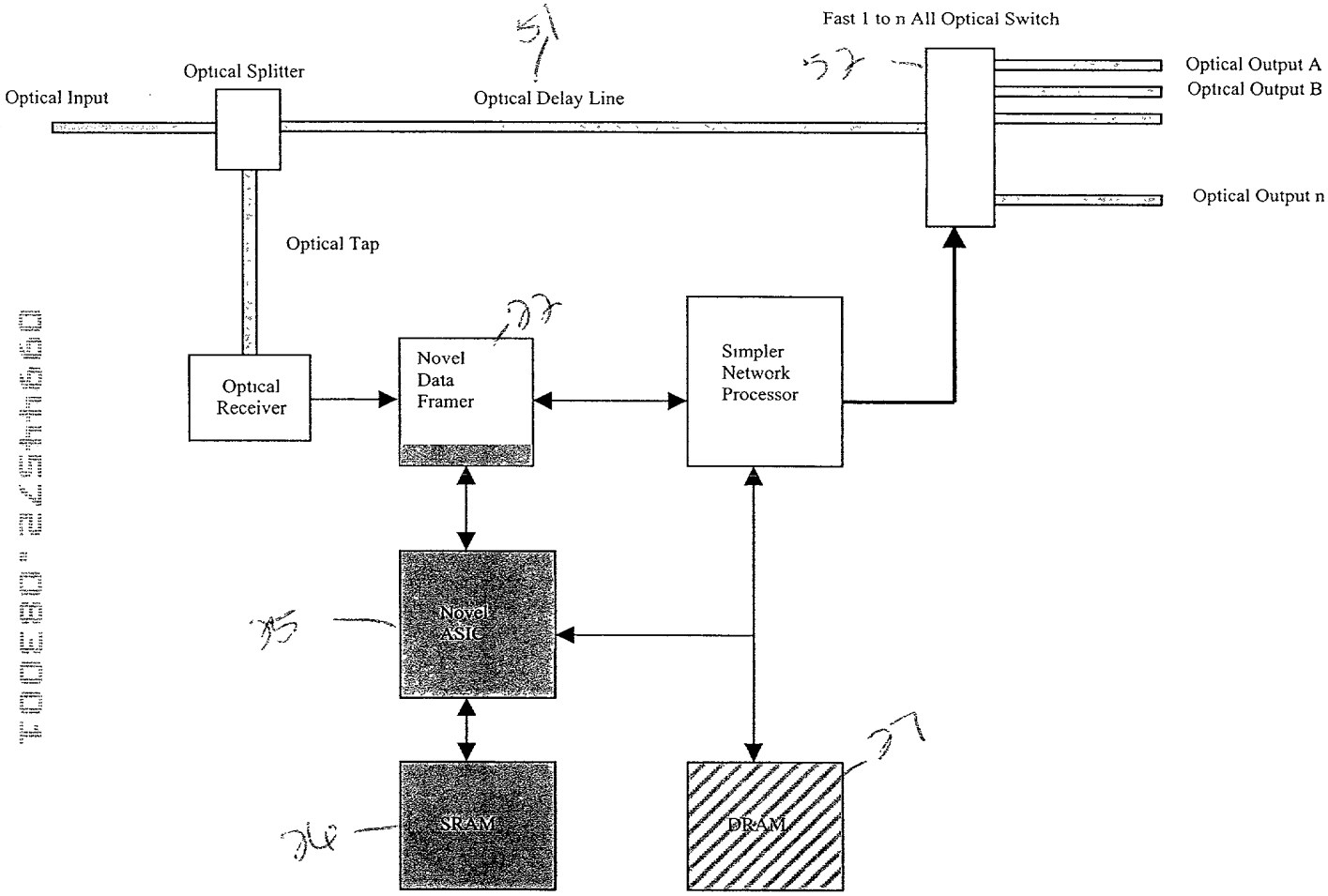
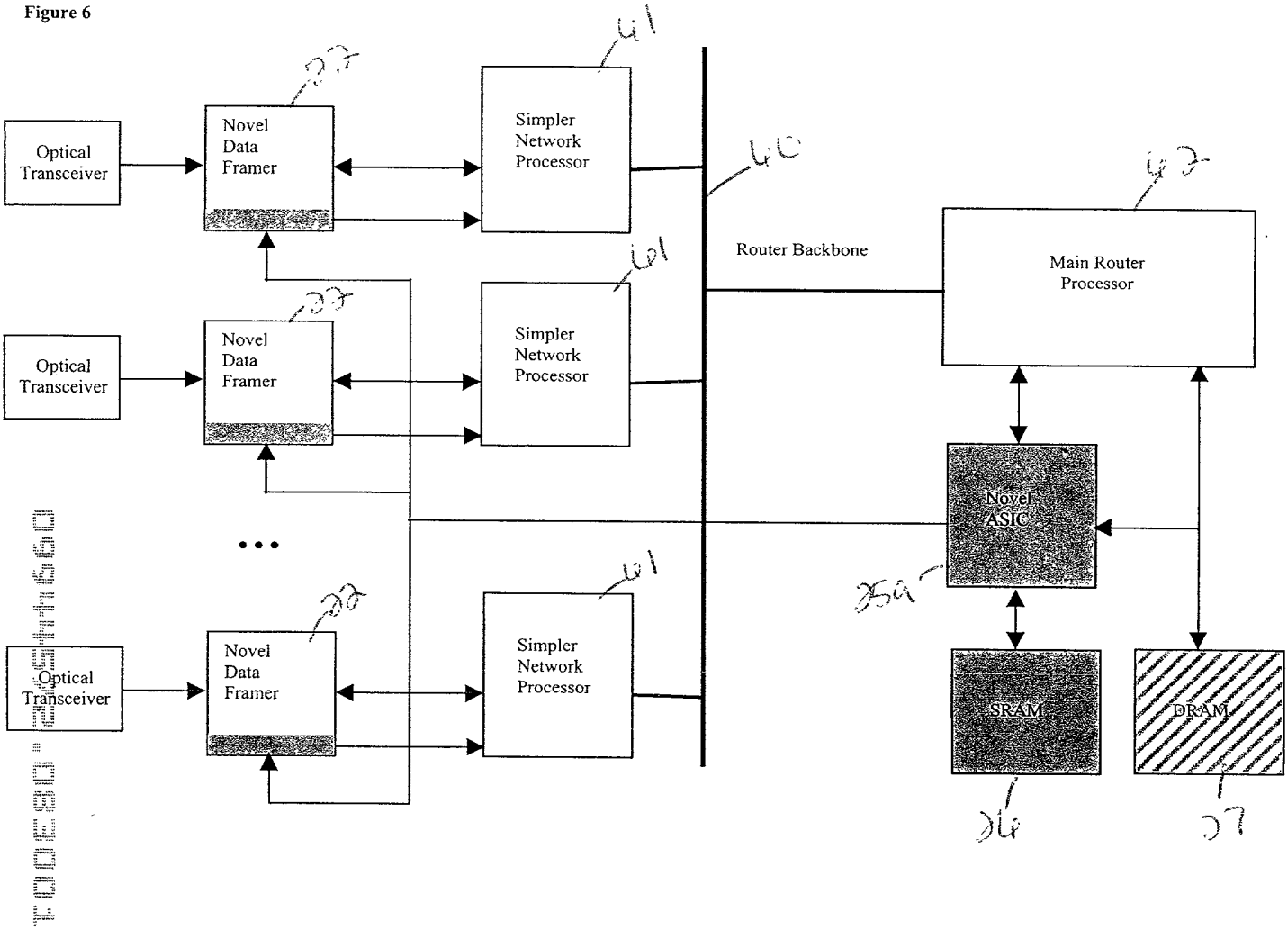
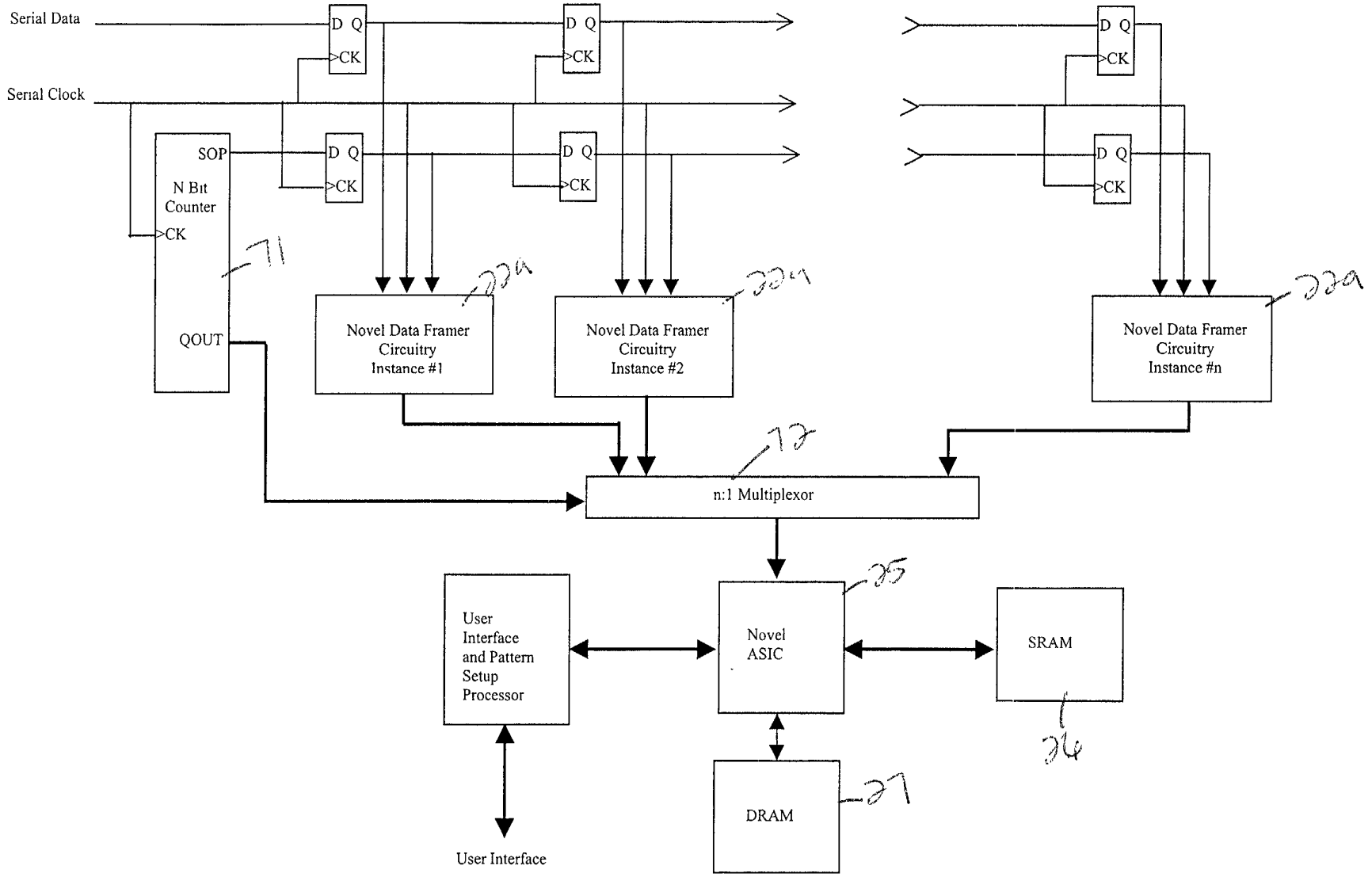

Fast 1 to n All Optical Switch
Optical Splitter
Optical Input
Optical Delay Line
Optical Output A
Optical Output B
Optical Output n
Optical Tap
Optical Receiver
Novel Data Framer
Simpler Network Processor
Novel ASIC
SRAM
DRAM

Figure 6


Optical Transceiver
Novel Data Framer
Simpler Network Processor
Router Backbone
Main Router Processor
Optical Transceiver
Novel Data Framer
Simpler Network Processor
Novel ASIC
Optical Transceiver
Novel Data Framer
Simpler Network Processor
SRAM
DRAM

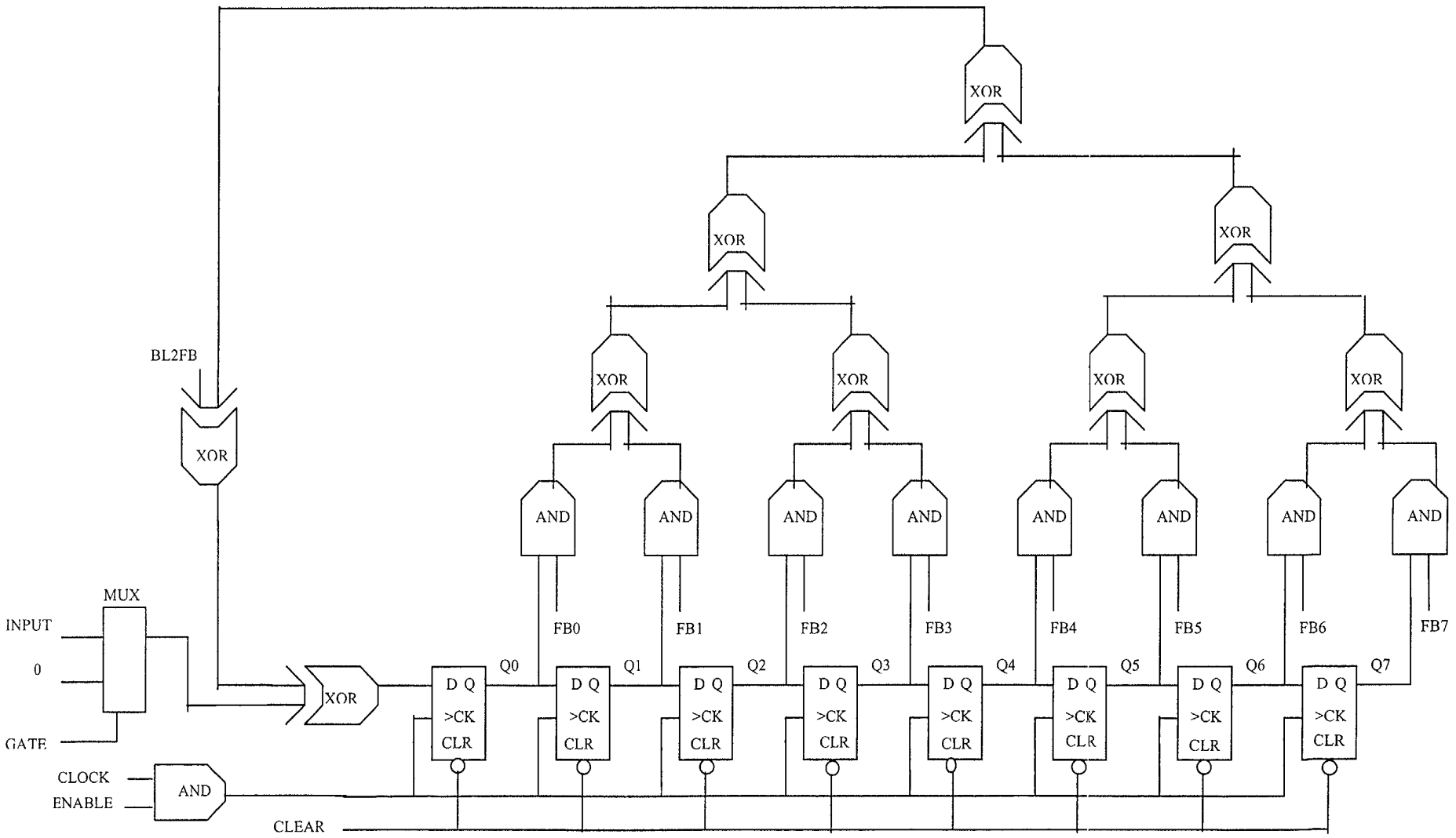
T00E80" 2Z5hm66D

Figure 7



T00280 "2Sth660

Figure 8a



T00280 25th660

Figure 8b

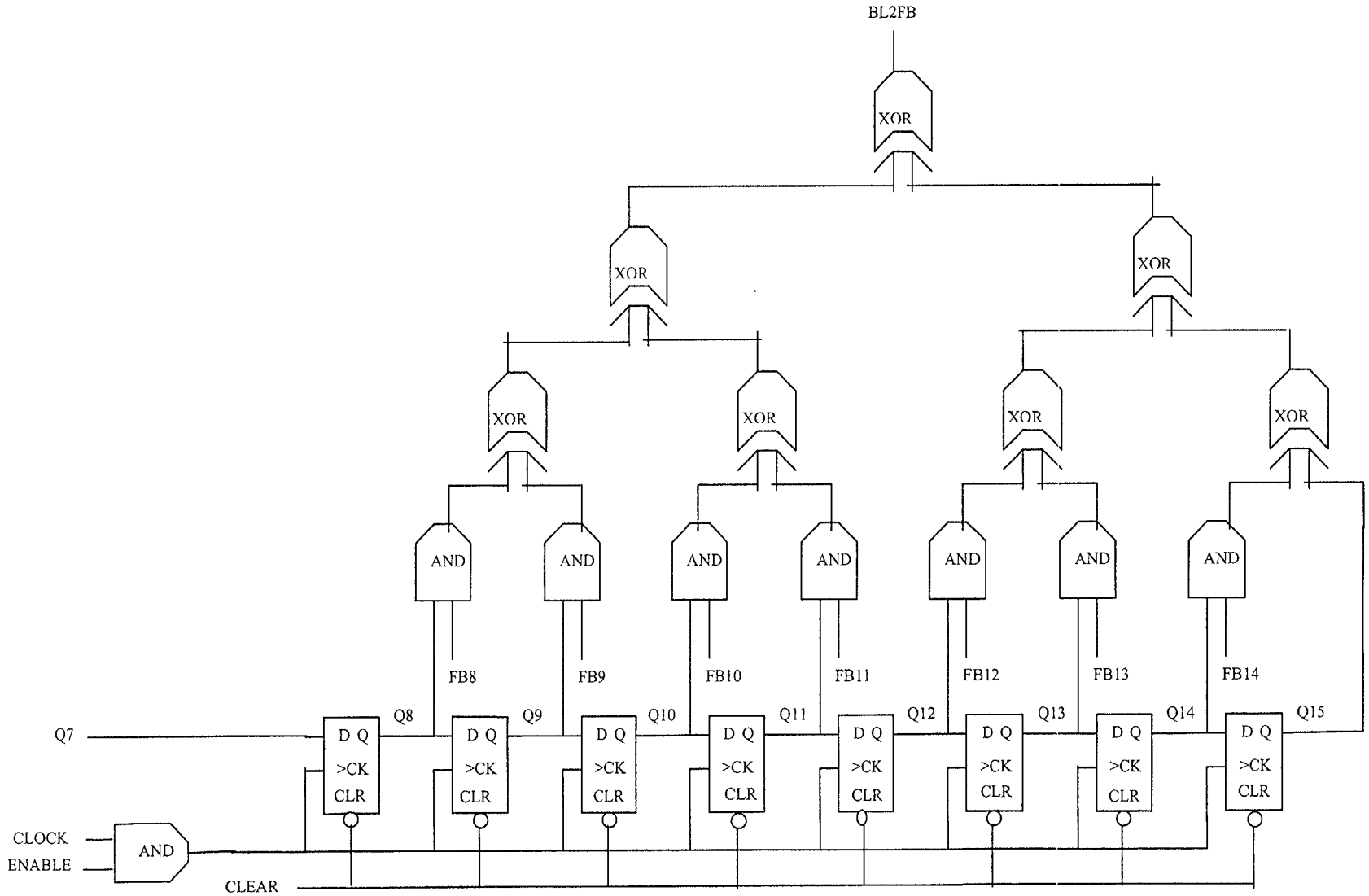


Figure 9

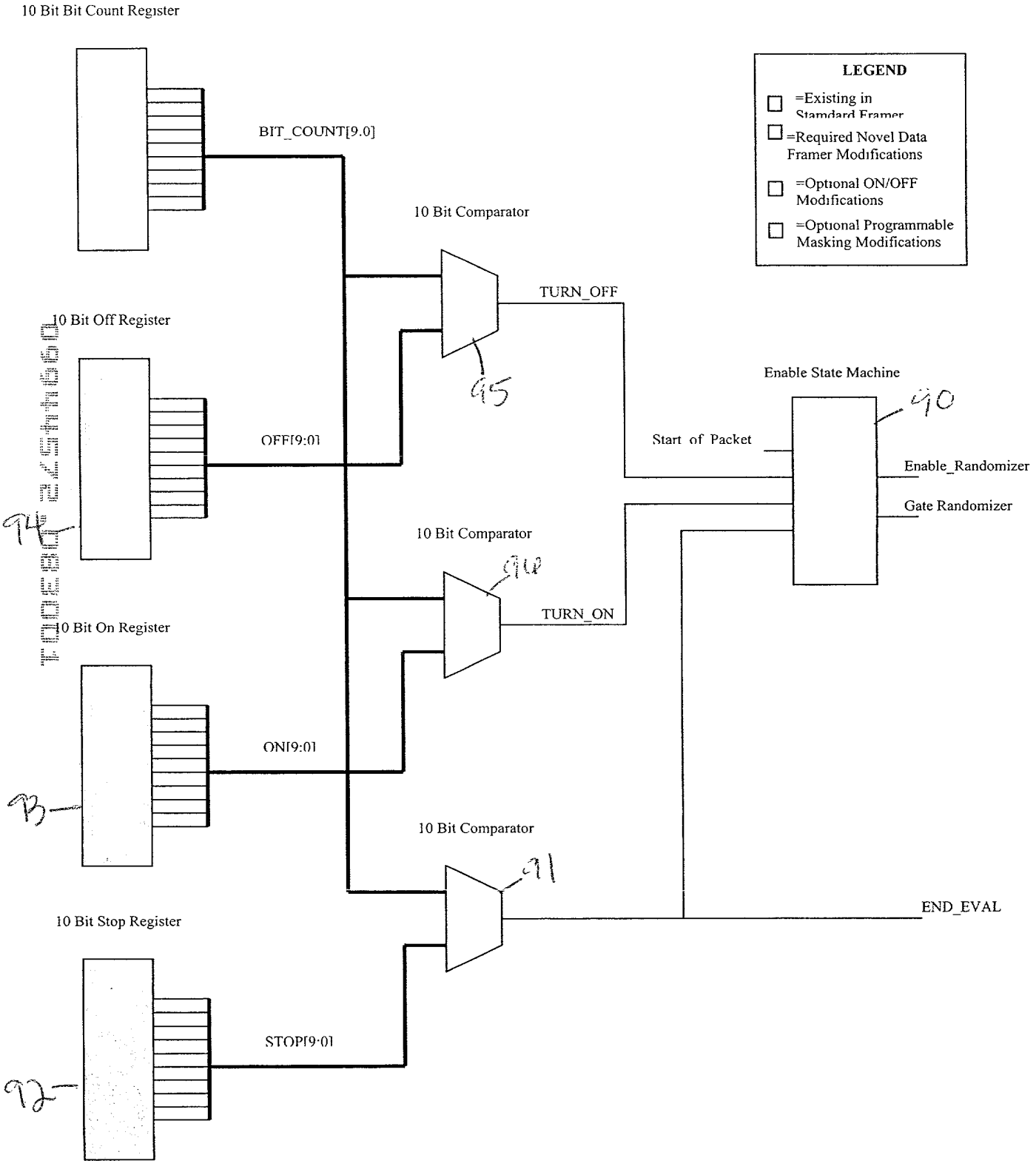

10 Bit Bit Count Register
BIT_COUNT[9.0]
LEGEND
=Existing in Standard Framer
=Required Novel Data Framer Modifications
=Optional ON/OFF Modifications
=Optional Programmable Masking Modifications
10 Bit Comparator
TURN_OFF
95
10 Bit Off Register
OFF[9:0]
Enable State Machine
90
Start of Packet
Enable_Randomizer
Gate Randomizer
10 Bit Comparator
92
TURN_ON
10 Bit On Register
ON[9:0]
10 Bit Comparator
91
END_EVAL
10 Bit Stop Register
STOP[9:0]

Figure 10

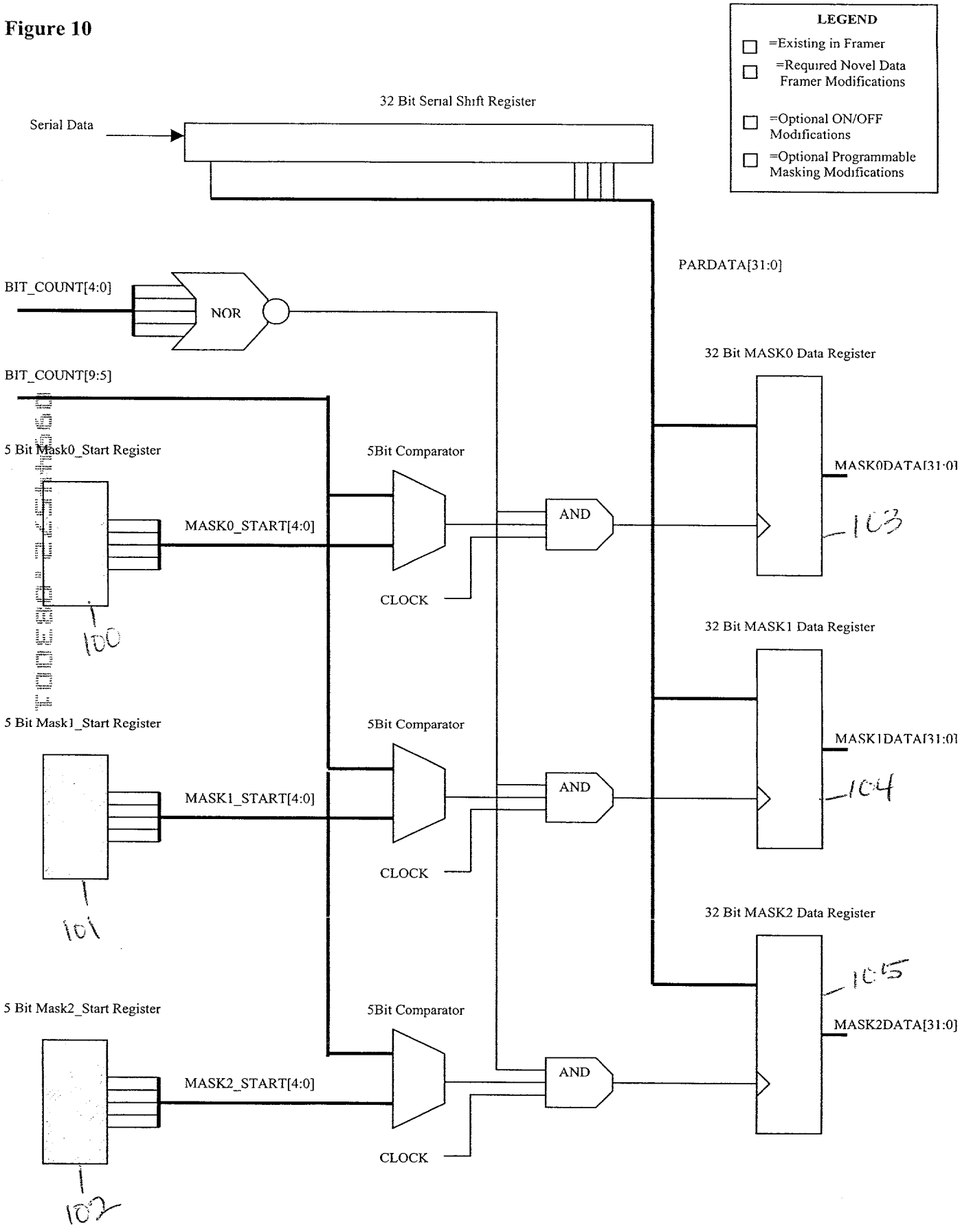

LEGEND
=Existing in Framer
=Required Novel Data Framer Modifications
=Optional ON/OFF Modifications
=Optional Programmable Masking Modifications
32 Bit Serial Shift Register
Serial Data
PARDATA[31:0]
BIT_COUNT[4:0]
NOR
BIT_COUNT[9:5]
32 Bit MASK0 Data Register
5 Bit Mask0_Start Register
5Bit Comparator
MASK0DATA[31:0]
MASK0_START[4:0]
AND
CLOCK
100
103
32 Bit MASK1 Data Register
5 Bit Mask1_Start Register
5Bit Comparator
MASK1DATA[31:0]
MASK1_START[4:0]
AND
CLOCK
101
104
32 Bit MASK2 Data Register
105
5 Bit Mask2_Start Register
5Bit Comparator
MASK2DATA[31:0]
MASK2_START[4:0]
AND
CLOCK
102

Figure 11

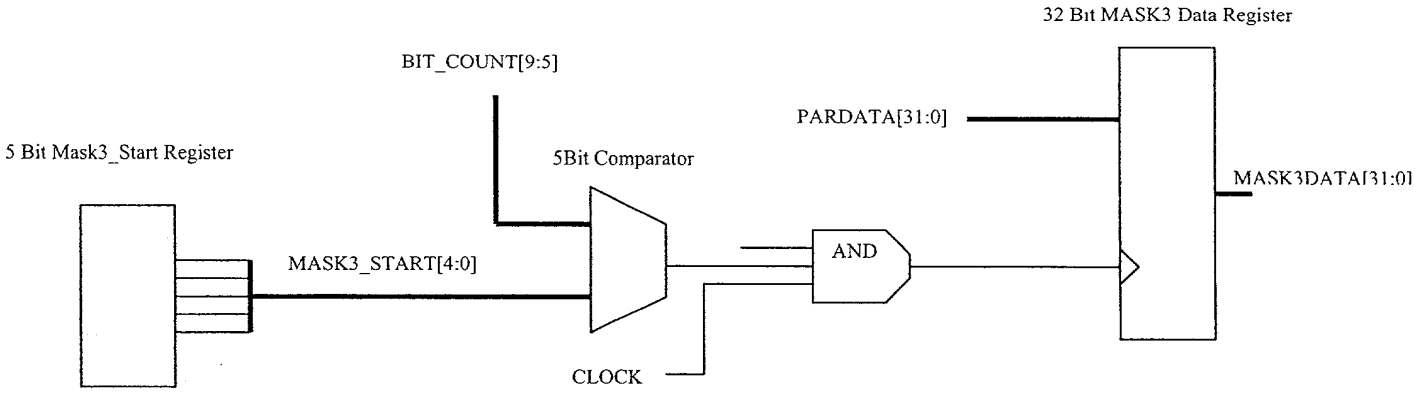

32 Bit MASK3 Data Register
BIT_COUNT[9:5]
PARDATA[31:0]
5 Bit Mask3_Start Register
5Bit Comparator
MASK3DATA[31:0]
MASK3_START[4:0]
AND
CLOCK

Figure 12

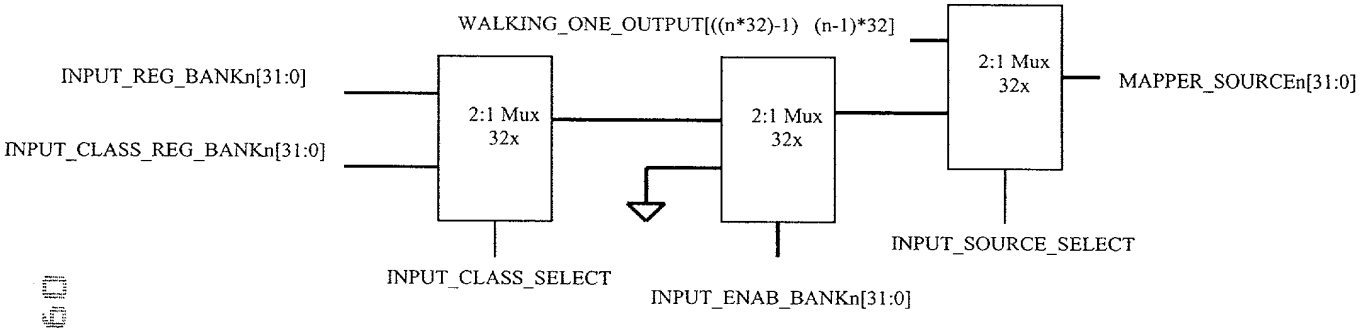

WALKING_ONE_OUTPUT[((n*32)-1) (n-1)*32]
INPUT_REG_BANKn[31:0]
INPUT_CLASS_REG_BANKn[31:0]
2:1 Mux
32x
2:1 Mux
32x
2:1 Mux
32x
MAPPER_SOURCEn[31:0]
INPUT_CLASS_SELECT
INPUT_ENAB_BANKn[31:0]
INPUT_SOURCE_SELECT

Figure 13

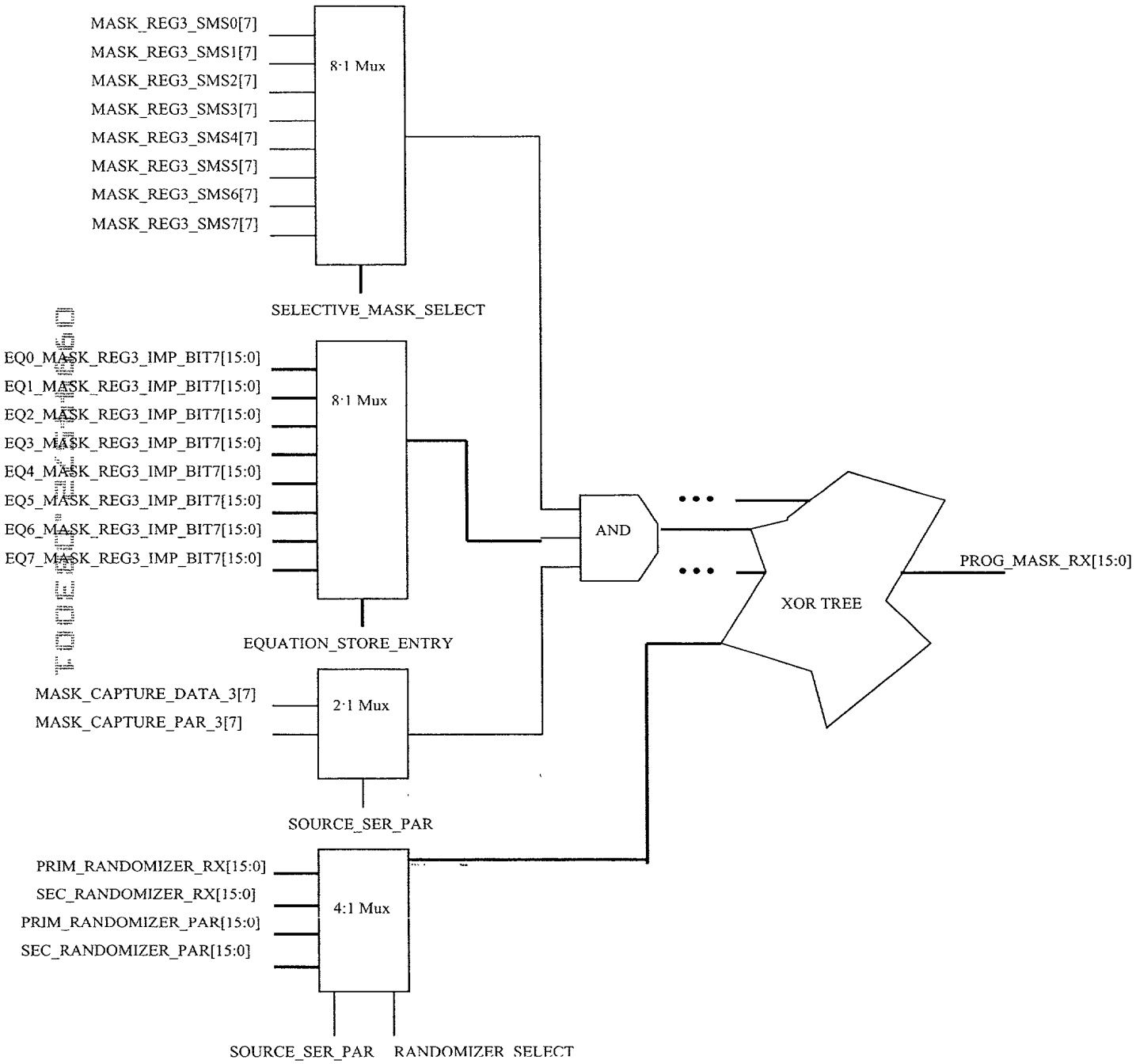

MASK_REG3_SMS0[7]
MASK_REG3_SMS1[7]
MASK_REG3_SMS2[7]
MASK_REG3_SMS3[7]
MASK_REG3_SMS4[7]
MASK_REG3_SMS5[7]
MASK_REG3_SMS6[7]
MASK_REG3_SMS7[7]
8:1 Mux
SELECTIVE_MASK_SELECT
EQ0_MASK_REG3_IMP_BIT7[15:0]
EQ1_MASK_REG3_IMP_BIT7[15:0]
EQ2_MASK_REG3_IMP_BIT7[15:0]
EQ3_MASK_REG3_IMP_BIT7[15:0]
EQ4_MASK_REG3_IMP_BIT7[15:0]
EQ5_MASK_REG3_IMP_BIT7[15:0]
EQ6_MASK_REG3_IMP_BIT7[15:0]
EQ7_MASK_REG3_IMP_BIT7[15:0]
8:1 Mux
EQUATION_STORE_ENTRY
AND
XOR TREE
PROG_MASK_RX[15:0]
MASK_CAPTURE_DATA_3[7]
MASK_CAPTURE_PAR_3[7]
2:1 Mux
SOURCE_SER_PAR
PRIM_RANDOMIZER_RX[15:0]
SEC_RANDOMIZER_RX[15:0]
PRIM_RANDOMIZER_PAR[15:0]
SEC_RANDOMIZER_PAR[15:0]
4:1 Mux
SOURCE_SER_PAR
RANDOMIZER_SELECT

Figure 14

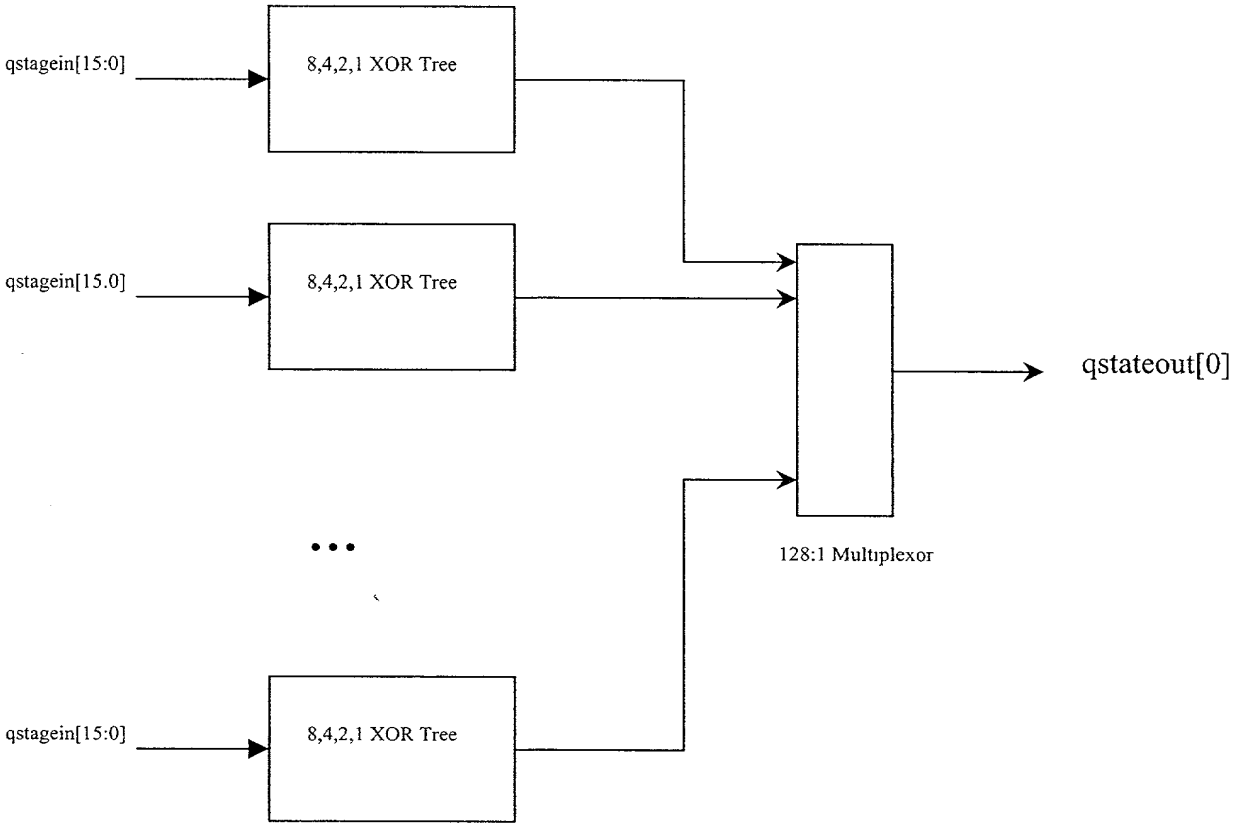

qstagein[15:0]
8,4,2,1 XOR Tree
qstagein[15.0]
8,4,2,1 XOR Tree
qstateout[0]
128:1 Multiplexor
qstagein[15:0]
8,4,2,1 XOR Tree

Figure 15

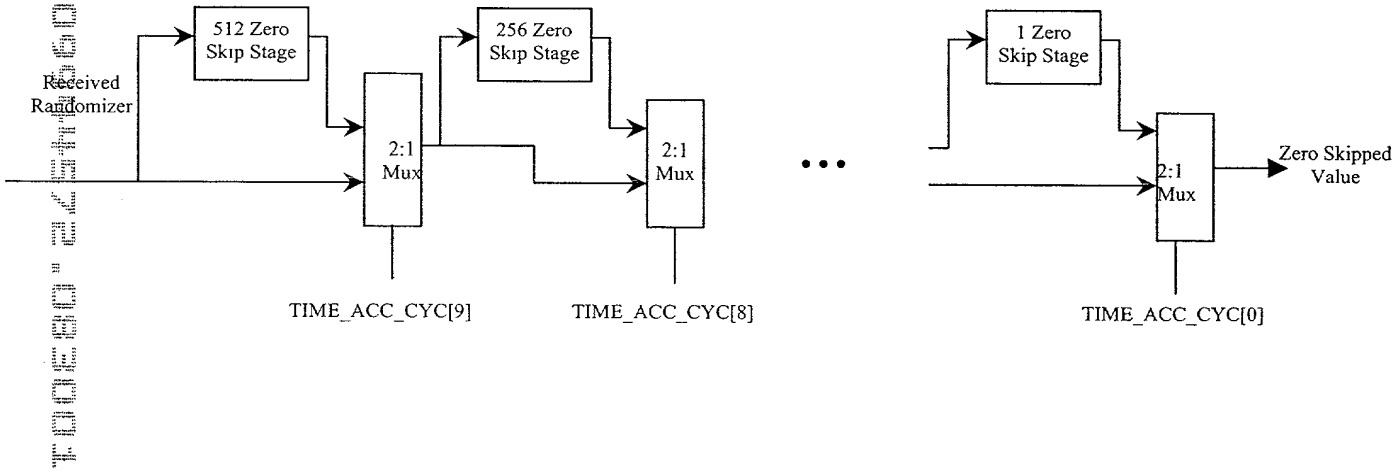

Received Randomizer
512 Zero Skip Stage
256 Zero Skip Stage
1 Zero Skip Stage
2:1 Mux
2:1 Mux
2:1 Mux
Zero Skipped Value
TIME_ACC_CYC[9]
TIME_ACC_CYC[8]
TIME_ACC_CYC[0]

Figure 16

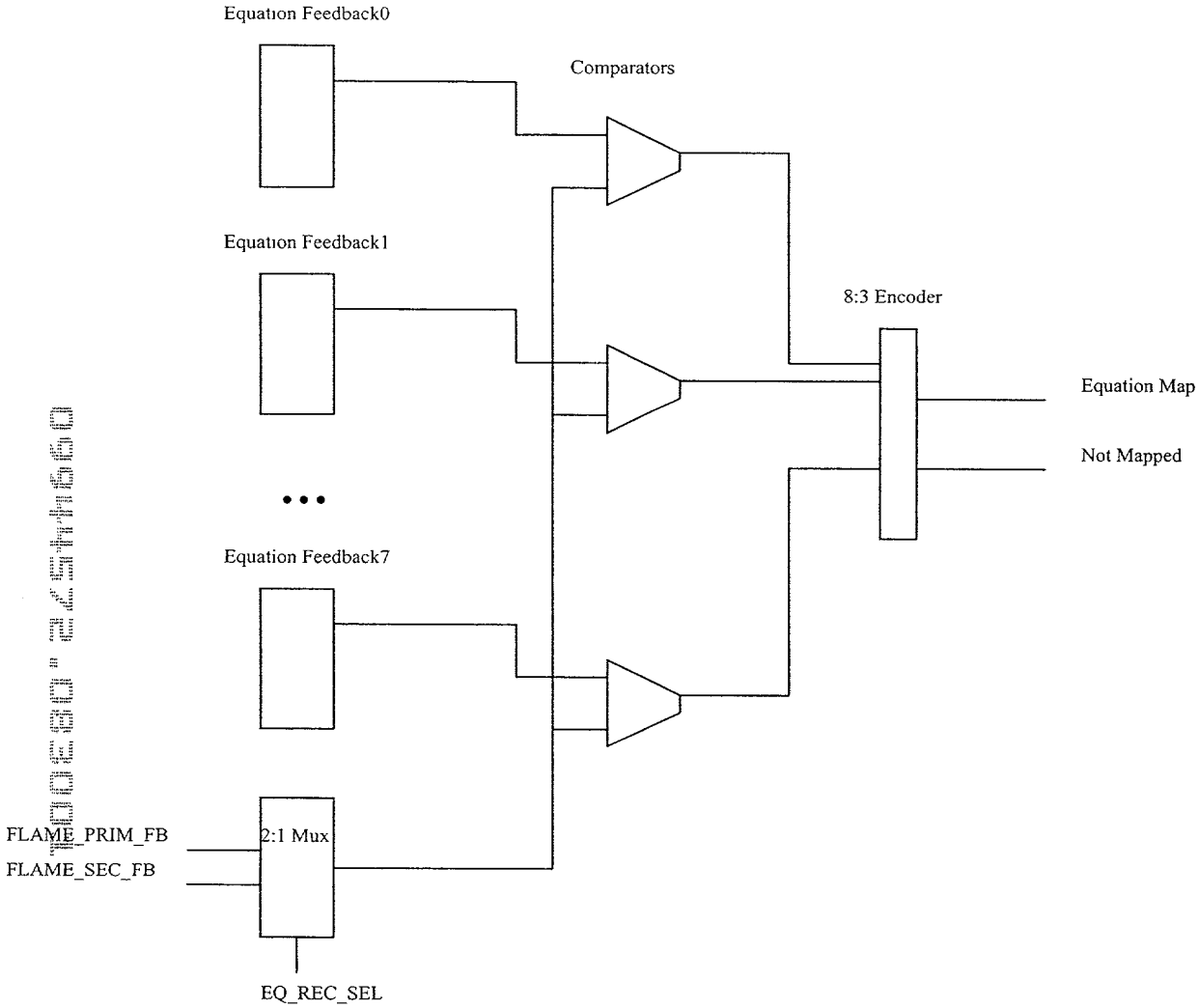

Equation Feedback0
Comparators
Equation Feedback1
8:3 Encoder
Equation Map
Not Mapped
Equation Feedback7
FLAME_PRIM_FB
FLAME_SEC_FB
2:1 Mux
EQ_REC_SEL

Figure 17

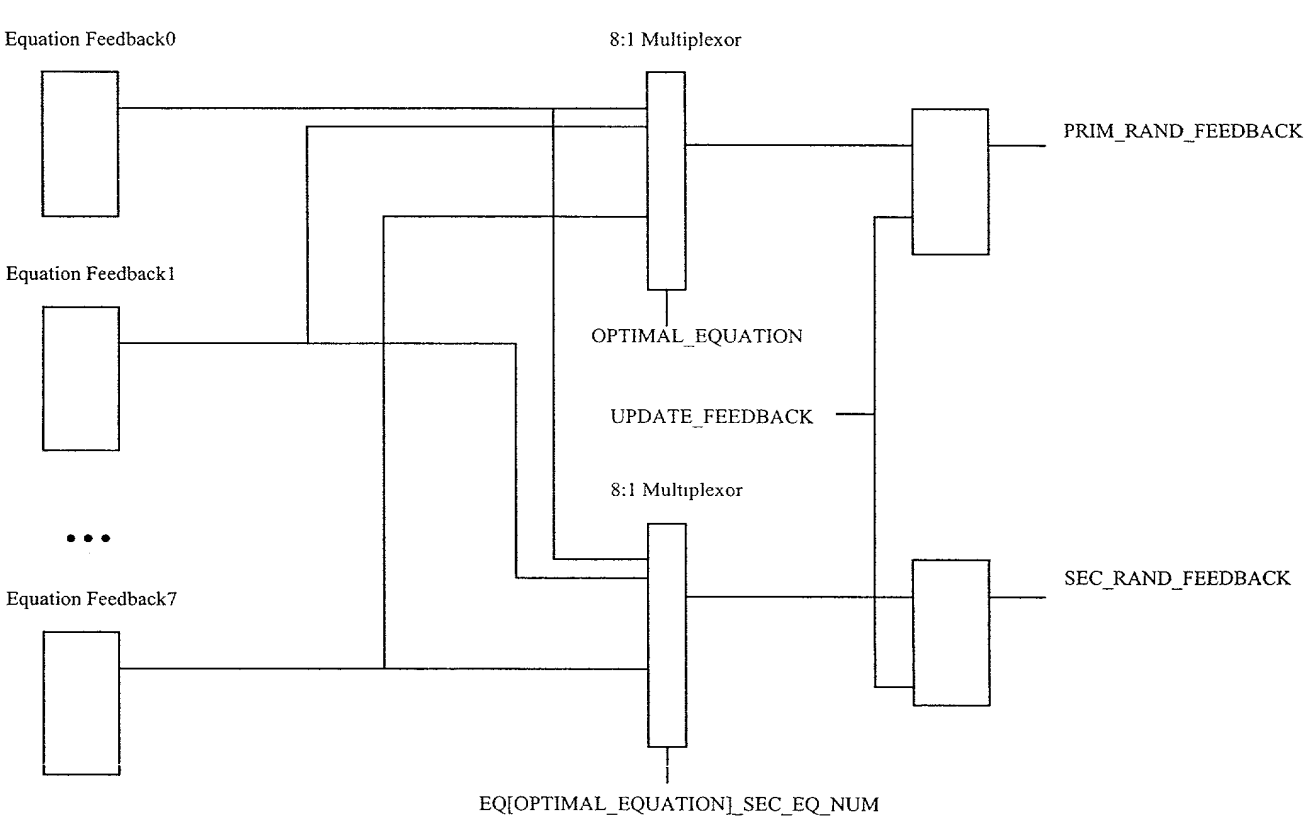

Equation Feedback0
8:1 Multiplexor
PRIM_RAND_FEEDBACK
Equation Feedback1
OPTIMAL_EQUATION
UPDATE_FEEDBACK
8:1 Multiplexor
SEC_RAND_FEEDBACK
Equation Feedback7
EQ[OPTIMAL_EQUATION]_SEC_EQ_NUM

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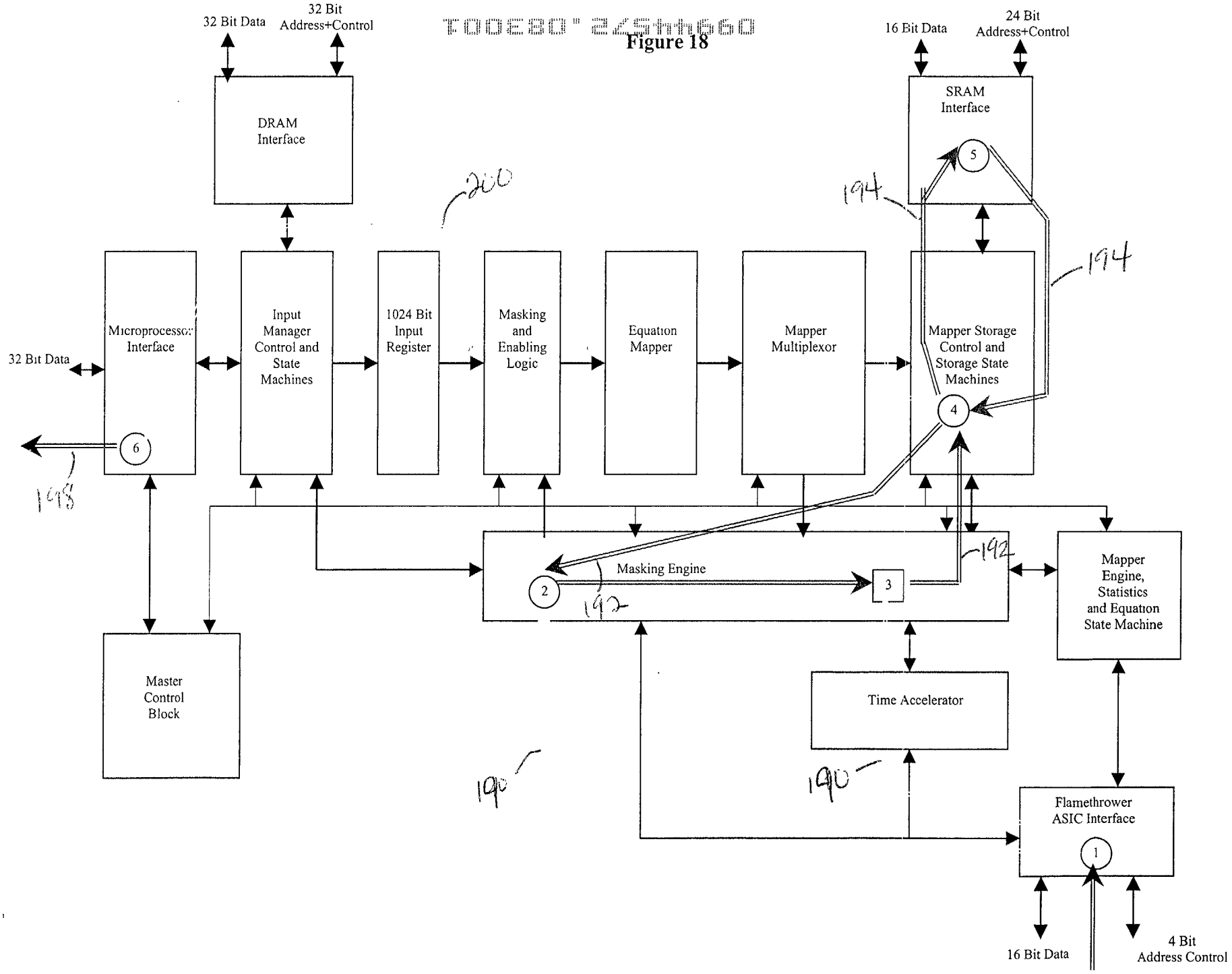
Figure 18



T00280 "27Shm660

Figure 19

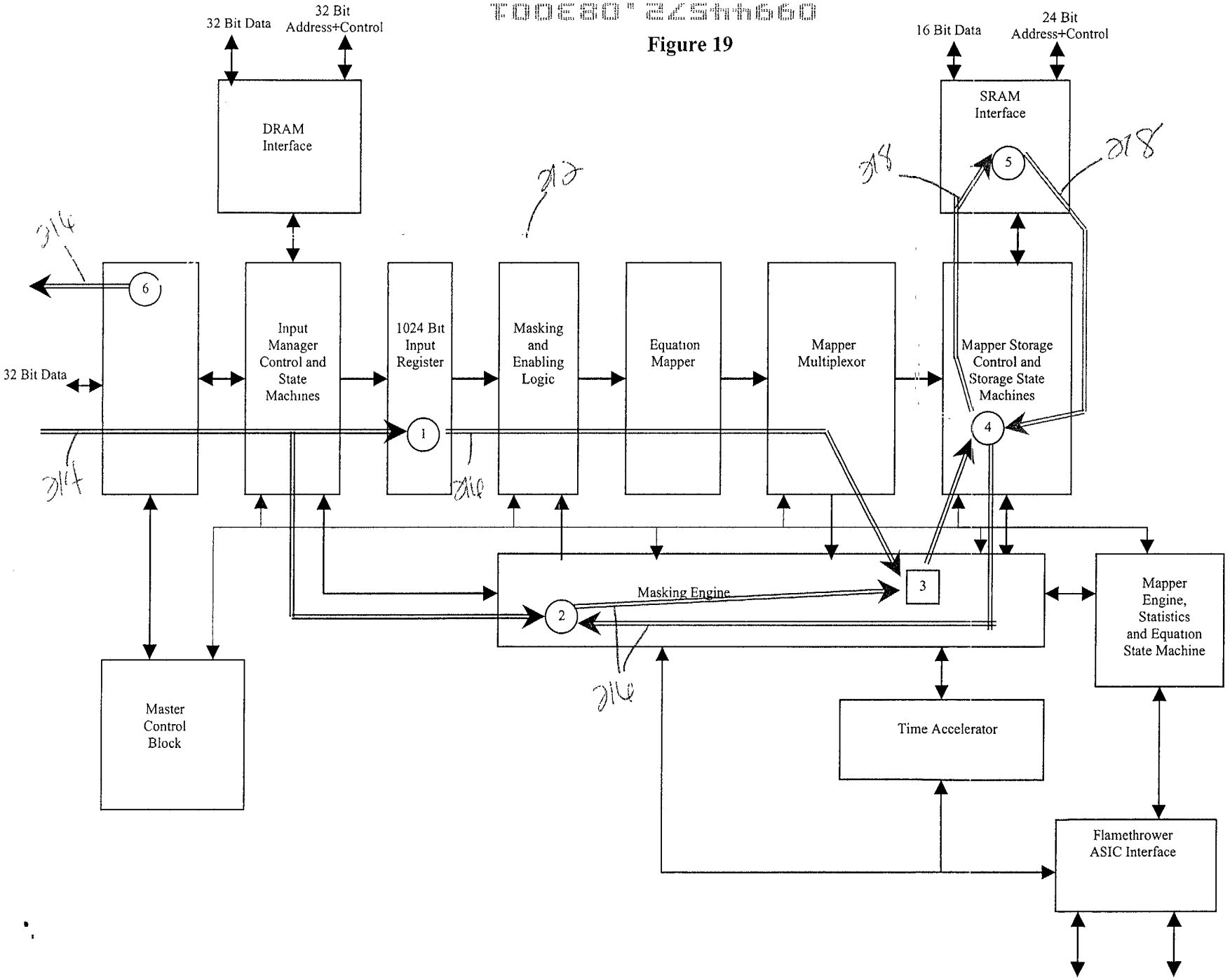
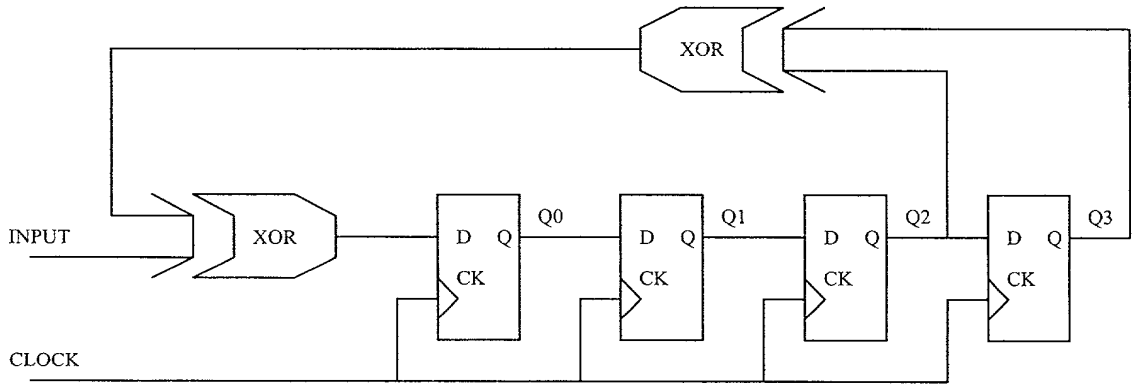



Figure 20 (Prior Art)